REMARKS

The specification has been carefully reviewed again, and minor errors have been corrected by this amendment in order to place the application in best condition for allowance.

Claims 1, 3 and 4 are to be replaced by claims 5, 6 and 7, respectively, in order to improve the form of those claims for purposes of allowance or, in the alternative, to place the claims in better condition for appeal. No new issues are raised since claims 5, 6 and 7 are merely improved versions of claims 1, 3 and 4 which they replace.

The disclosed and claimed invention is directed to a voice transceiver which, in its basic form as shown in Figure 1, comprises an input decoding code buffer 301 which receives and temporarily stores compressed voice codes, and a voice decoder 401 connected to and triggered by input decoding code buffer for expanding the compressed voice codes and generating digitalized digital voice data. The invention further comprises a selective disposal unit 200 which receives the generated digitalized digital voice data from the voice decoder. This selective disposal unit 200 is responsive to a discard request for discarding the generated digitalized digital voice data when the discard request is present. Generated digitalized digital voice data which has not been discarded is temporarily stored in a speaker output buffer 501. An insertion/disposal control unit 100 monitors data temporarily stored in the speaker output buffer 501, and if an amount of data temporarily stored in the speaker output buffer falls below a first threshold, the insertion/disposal unit 100 outputs a dummy voice code to the decoding code buffer 301. However, if an amount of data temporarily stored in said speaker output buffer 501 rises above a second threshold, the insertion/disposal unit 100 generates the discard request to the selective disposal unit 200, causing that unit to dispose of generated digitalized digital voice data from the voice decoder 401. A digital-to-analog converter 601 converts the generated digitalized digital voice data temporarily stored in said speaker output buffer 501 to an analog voice signal,

which is amplified by amplifier 701 and applied to a speaker 801.

Since the amount of digital voice data stored in the speaker output buffer 501 is monitored and dummy code is inserted when the amount of data in the speaker buffer falls below a first threshold, the voice transceiver smoothly outputs an output voice from the speaker without breakup in the output voice. When the dummy code is input to the decoding code buffer 301, the strength of the compressed voice code input immediately prior to the dummy code is reduced. Also, by preventing overflow of the speaker output buffer though control of the selective disposal unit 200, the transceiver again smoothly outputs an output voice from the speaker without breakup of the output voice.

The embodiment shown in Figure 2 adds to this basic configuration. This embodiment adds a microphone 802 for inputting an acoustical voice input and an amplifier 702 for amplifying the voice signal from the microphone, an analog-to-digital converter 602 for converting said voice signal into digital voice data, and a microphone buffer 502 for receiving and temporarily storing the converted digital voice data. This embodiment further adds a reference input signal buffer 901 for receiving and temporarily storing generated digitalized digital voice data passed by the selective disposal unit 200. In other words, the reference input signal buffer 901 stores the same information as the speaker output buffer 501. The insertion/disposal control unit 100 is connected to said reference signal buffer unit 901 to thereby monitor data temporarily stored in the speaker output buffer 501. An acoustic echo canceller 902 is responsive to the reference input signal buffer 901 to suppressing an echo component contained in the converted digital voice data output from the microphone buffer 502. A voice encoder 402 is connected to receive converted digital voice data from the acoustic echo canceller 902 and encodes and compresses an output voice code.

Claims 1 and 3 and their replacements, claims 5 and 6, are directed to the basic embodiment shown in Figure 1. Claim 4 and its replacement, claim 7, is directed to the embodiment shown in Figure 2.

Claims 1 and 3 were rejected under 35 U.S.C. §103(a) as being

unpatentable over U.S. Patent No. 5,526,353 to Henley et al. in view of U.S. Patent No. 4,618,936 to Shiono in further view of U.S. Patent No. 4,993,022 to Kondo et al. This rejection is respectfully traversed for the reason that the combination of Henley et al., Shiono and Kondo et al. does not result in the claimed invention, nor is there any teaching that can be derived from this combination that would suggest the claimed invention.

The patent to Henley et al. discloses a system and method for communicating audio data in a packet-based computer network wherein transmission of data packets through the computer network requires variable periods of transmission time. The system comprises: (1) a packet assembly circuit for constructing a data packet from a portion of a stream of digital audio data corresponding to an audio signal, the packet assembly circuit generating a position identifier indicating a temporal position of the portion relative to the stream, inserting the position identifier into the data packet and queuing the data packet for transmission through a backbone of the computer network and (2) a packet disassembly circuit, having a buffer associated therewith, for receiving the data packet from the backbone, the packet disassembly circuit inserting the portion into an absolute location of the buffer, the position identifier determining the location, the portion thereby synchronized with adjacent portions of the stream of digital audio data in the buffer to compensate for the variable periods of transmission time. Henley et al. state that the purpose of their invention is to compensate for variable packet transmission times (jitter) that occurs in transmitting and receiving digitized audio data in a packet-based computer network.

Figure 1 of Henley et al. illustrates a computer network 100 that includes a telephone instrument 110 coupled, via a PC 120 having a display screen 124, to an Ethernet-type computer network backbone 130. Other telephone instruments 112, 114 may be coupled to the backbone 130 via a multiple station card 122. The Henley et al. system is capable of transmitting audio signals among the telephone instruments 110, 112, 114 via the Ethernet backbone 130. The Ethernet backbone 130 is linked through an Ethernet Switch 140 and an ATM hub 150 to a Token

Ring backbone 172 of a Token Ring LAN 170. The Token Ring backbone 172 is coupled, via a PC 176 having a display screen 178, to a telephone instrument 174. The ATM hub 150 is coupled, via a PC 154 to a display screen 156, to a telephone instrument 154. Packetized computer data transmitted across the Ethernet backbone 130 is switched through the Ethernet switch 140 to the ATM hub 150. Packetized computer data transmitted across the Token Ring backbone 172 is routed directly through the ATM hub 150. A telephone server 160 is connected to a plurality of telephone instruments 162, 164 and connected, via the Ethernet Switch 140, to the Ethernet backbone 130. The telephone server 160 is also connected through the ATM hub 150. Audio data from the Ethernet backbone 130 is directed through the telephone server 160, via the Ethernet switch 140, to the ATM hub 150. The telephone server 160 provides full ISDN communication to central office trunk lines 166, thereby allowing WAN via ATM. In the illustrated embodiment, the telephone server 160 multiplexes signals from dedicated telephones 162, 164 and audio data from the backbone 130 of the Ethernet physical protocol layer, thereby providing digital service of audio data.

Figure 2 of Henley et al. illustrates a block diagram of a microprocessor-based system which comprises a microprocessor 210, a digital signal processor ("DSP") 220, a CODEC 230, a telephone set interface 240, a connector 242, random-access memory ("RAM") 250, an Ethernet controller 260, an Ethernet controller interface connector 262, a dual port memory 270, and a dual port memory interface connector 272. Standard telephone instrument 110 connectivity is provided into the PC 120 through the telephone set interface 240 and connector 242. The telephone set interface 240 accepts an analog signal from the telephone instrument 110 and is preferably a standard RJ-11 connector. The telephone set interface 240 is coupled to the CODEC 230. The CODEC 230 provides the analog-to-digital and digital-to-analog conversion for the audio data. The CODEC 230 comprises a digital conversion/compression circuit for digitizing and compressing the audio signal into the stream of digital audio data. Those of ordinary skill in the art should understand that the present invention does not

depend upon application of a particular compression/decompression algorithm, or upon whether the data are even compressed at all. When the telephone instrument 110 transmits an analog audio signal to the CODEC 230, the CODEC 230 samples the signal at a predetermined, conventional rate of 8kHz. The CODEC 230 then preferably employs a known, standard logarithmic compression method to compress a 13 or 14 bit wide data sample into an 8 bit compressed sample. The CODEC 230 further comprises a decompression/analog conversion circuit for decompressing and converting the stream of digital audio data back into the audio signal. The decompression circuit restores the 8 bit compressed sample into a decompressed 13 or 14 bit sample and converts the sample into an analog voltage for reproduction in the telephone instrument 110. Finally, the CODEC 230 has an associated clock (not illustrated) that governs the pace of the CODEC's operation. The DSP 220 analyzes, filters and enhances audio data from the CODEC 230. The DSP 220 may also provide echo cancellation or compression/decompression in lieu of the CODEC 230. Echo cancellation is typically a requirement when the round trip audio delay exceeds 60 ms. The processor 210 is charged with the responsibility of compiling the information from the DSP 220 and Ethernet controller 260 and performing the operations required to transmit the data. The processor 210 therefore embodies the packet assembly circuit and the packet disassembly circuit. The packet assembly circuit generates a position identifier 370 that indicates a temporal position of the portion relative to the stream, inserts the position identifier 370 into the data packet and queues the data packet in the Ethernet controller for transmission through the Ethernet backbone 130. The processor 210 further embodies an interpolation circuit for inserting synthesized audio data into a designated location of the receiving buffer 510 (Figure 5) to thereby lengthen the portions of the stream of audio data in the receiving buffer 510 and a decimation circuit for deleting audio data from a designated location of the receiving buffer 510 to thereby shorten the portions of the stream of audio data in the receiving buffer 510. Access between the dual port memory 270 and the I/O bus 280 of the PC 120 is provided through the dual port memory connector 272.

The dual port memory 270 provides storage capacity and overflow back-up in facilitating communication between the internal local bus 265 and the I/O bus 280. Digital data from the Ethernet controller 260 and the processor 210 can be stored in the dual port memory 270.

The Examiner's analysis of claim 1 paraphrases the claim and attributes to Henley et al. the following:

- "a voice transceiver . . . analog data" as compressed codes (col. 10, lines 9–11). What new claim 5 (corresponding to claim 1) recites is "input means for receiving and temporarily storing compressed voice codes". This corresponds to the decoding code buffer 301 of the drawings of this application. What the cited passage of Henley et al. states is "When the telephone instrument 110 transmits an analog audio signal to the CODEC 230, the CODEC 230 samples the signal at a predetermined, conventional rate of 8kHz."
- "an expansion means . . . digital voice data" as expanding compressed data (col. 10, lines 12–15). What new claim 5 recites is "voice decoder means connected to and triggered by said input means for expanding the compressed voice codes and generating digitalized digital voice data". This corresponds to the voice decoder 401 of the drawings of this application. What the cited passage of Henley et al. states is "The CODEC 230 then preferably employs a known, standard logarithmic compression method (such as A-Law or μ-Law) to compress a 13 or 14 bit wide data sample into an 8 bit compressed sample."
- "a buffer . . . voice data" as dual port memory (col. 10, lines 54–58). What new claim 5 recites is "speaker output buffer means for receiving and temporarily storing digitalized digital voice data passed by said selective disposal means". The recited speaker output buffer means corresponds to the SP output buffer 501 of the drawings of this application. Note that this is not necessarily a "dual port memory" and is not recited as such as would seem to be implied by the Examiner. What the cited passage of Henley et

al. states is "Access between the dual port memory 270 and the I/O bus 280 of the PC 120 is provided through the dual port memory connector 272. The dual port memory 270 provides storage capacity and overflow back-up in facilitating communication between the internal local bus 265 and the I/O bus 280." Note that the dual port memory 270 of Henley et al. is not a speaker output buffer and does not serve that purpose. Note also that there is no "selective disposal means", as recited in the claim, which passes data to be buffer.

- "a conversion means . . . said detection signal . . . and speaker means for emitting said analog voice data into the air" as converting data back to analog for listener (col. 7, lines 27–33). What new claim 5 recites is "digital-to-analog converter means for converting the generated digitalized digital voice data temporarily stored in said speaker output buffer means to an analog voice signal; and a speaker connected to receive said analog voice signal and generating an acoustical output." These correspond to D/A converter 601 and speaker 801 shown in the figures of this application. What the cited passage of Henley et al. states is "In a preferred embodiment of the present invention, the system further comprises a decompression/analog conversion circuit, coupled to the packet disassembly circuit, for decompressing and converting the stream of digital audio data back into the audio signal. Thus, the received audio data are converted into a medium that the listener on the receiving end can understand and respond to in kind."

The Examiner goes on to assert, again by paraphrasing the claim 1, that Henley et al. teaches "further comprising a data control means for controlling . . . based on said detection signal, wherein said data control means outputs a dummy code . . . buffer means is less than a required amount . . . when said buffer means approaches an overflow amount . . . does not allow the output of said digital voice data to said conversion means" as inserting white noise when there is not enough

data and decimation when there is too much data (col. 15, lines 7–46). What new claim 5 recites is "insertion/disposal control means connected to monitor data temporarily stored in said speaker output buffer means and, if an amount of data temporarily stored in said speaker output buffer means falls below a first threshold, outputting a dummy voice code to said input means, but if an amount of data temporarily stored in said speaker output buffer means rises above a second threshold, generating said discard request to said selective disposal means". Note that the recited insertion/disposal control means outputs a dummy voice code to the input means when the amount of data temporarily stored in the speaker output buffer is less than a first threshold and generates a discard request to the selective disposal means when the amount of data in the speaker output buffer is greater than a second threshold. However, as demonstrated above, there is no speaker output buffer and no selective disposal means in Henley et al. What the cited passage of Henley et al. states is

> "Sample 5 further illustrates the circumstance when a shortened audio data sample 380 is transmitted. Sample 5, which is only 24 bytes long, is inserted into the receiving buffer at PI_5 =73. Since sample 5 is short by 20 bytes, the missing 20 bytes are filled with white noise, representing silence. The silence is not shown, as will be explained.
>
> "Next sample 6 arrives. Sample 6 is a full-length packet of 44 bytes. Thus, PI_6 equals 79. Sample 6 overwrites the 20 bytes of silence that had been appended to the end of sample 5. Since FIG. 5 already shows sample 6 in place, the silence is already overwritten and thus not shown.
>
> "Finally, sample 7 displays the circumstance when the CODEC clock operates too slowly. For purposes of discussion, the CODEC clock is assumed to be grossly out of frequency, such that the effect produced thereby is emphasized. In such case, PI advances 5.5 ms or 11 positions from the previous PI to position 90 in the receiving buffer 510. However, the slow CODEC clock forces the CRO to lag. In this instance, the CRO only advances 5.0 ms or 10 positions from the previous CRO to position 60 in the receiving buffer 510. The result is that the length of the window is 20.5 ms. Decimation is therefore required to shorten the receiving buffer 510 to the pre-set size.
>
> "Decimation is performed in adjustment intervals as follows: 1 byte for every 2 bytes away from the ideal window

> length (160 bytes, in the illustrated embodiment), 2 bytes for every 3 or 4 bytes away from the ideal window length and 3 bytes for every 5 or 6 bytes away from the ideal window length. In this instance, the buffer is 0.5 ms too long, equating to 4 bytes. Accordingly, the decimation circuit must remove 2 bytes from the receiving buffer 510 to adjust the receiving buffer 510 window toward the ideal length. Interpolation and decimation are ongoing processes in the system of the present invention.
>
> "Before leaving FIG. 5, it should be noted that, if window length is reduced to zero (either by virtue of the non-transmission of periods of silence or by virtue of reception of multiple invalid packets), the CODEC 230 simply reads the white noise in the receiving buffer 510, thereby simulating silence, again for the benefit of the listener."

What Henley et al. describe is the process related to ATM packets, not what is essentially a continuous stream of voice code as is processed by the claimed invention.

The Examiner states that Henley et al. "does not *explicitly* teach detection means". The use of the adverb "explicitly" is misleading because it implies that there might be some *implicit* teaching in Henley et al. of this feature when, in fact, there is none. New claim 5 recites "insertion/disposal control means", as quoted in more detail above, and this "insertion/disposal control means" performs the "detection" function to which the Examiner has reference. The Examiner relies on Shiono for a teaching of the detection means.

The patent to Shiono dicloses an electronic cash register system includes an input keyboard and a high-speed computer which outputs through a buffer to a low-speed speech synthesizer. To avoid loss of data due to buffer overfill, a speech condition determination unit generates a control signal if the empty-condition of the buffer falls below a threshold. Note that Shiono is concerned with avoiding loss of data, whereas the claimed invention is not. Note also that Shiono is concerned with an entirely different system than that of either Henley et al. or the claimed invention.

The Examiner finds in the Shiono disclosure "a detection means . . . detection result" as when buffer is full and reassembly of data when acquired

(Fig. 5, subblocks 34, 36, 40, 62, 64, and 44; col. 4, line 10, – col. 6, line 65). The cited passage comprises a substantial portion of the Shiono patent, but a fair reading of the passage will reveal that it does not suggest the specifically recited "insertion/disposal control means". At col. 5, lines 3 to 14, Shiono describes the functions of the specifically cited subblocks as follows:

> "When the speech generation of the first speech data is completed, the detection circuit 60 develops the control signal to perform the read operation of the next speech data stored in the addresses 3 to 6 of the speech data buffer memory 36. When the speech data stored in the addresses 3 to 6 of the speech data buffer memory 36 is read out, the count contents stored in the speech generation pointer 62 reach '7'. In this way, the speech data (code signal) stored in the speech data buffer memory 36 is sequentially read out. The count contents stored in the speech generation pointer 62 indicate the address from which the next data should be read out."

This is not the function of the recited insertion/disposal control means as recited in new claim 5 (nor was it the function of the "detection means" recited in claim 1). Nevertheless, the Examiner incorrectly concludes that it would have been obvious to modify the teachings of Henley et al. "with a CPU monitoring of a buffer memory because it would advantageously allow the system to produce corresponding speech with data in a timely fashion". This statement is wholly unsupported by the combination of Henley et al. and Shiono, amounting in an unwarrented reconstruction of Henley et al. to produce a result that neither Henley et al. nor the claimed invention seek to achieve.

The Examiner goes on to state that the combination of Henley et al. and Shiono "does not *explicitly* teach a selective disposal unit for selectively discarding digital voice data". Again, the use of the adverb "explicitly" is misleading because it implies that there might be some *implicit* teaching in Henley et al. of this feature when, in fact, there is none. The Examiner relies on Kondo et al. for a teaching of "a technique to selectively discard data based on sound quality".

Kondo et al. disclose a system for and a method of multiplexing digital speech signals corresponding to speech signals inputted from a plurality of

terminals, the digital speech signals including a plurality of speech unit signals, in which a weighted priority signal is produced for the speech unit signal of each of the speech signals from the terminals, an assignment signal is produced from the priority signals indicative of which of the speech unit signals be selected for transmission in the form of a train of multiplexed speech unit signals in a cyclic transmission period of time, so that the speech unit signals are multiplexed on the basis of the assignment signal. The Examiner refers particularly to Figure 8 of Kondo et al. This figure is a block diagram illustrating a structure of a system for multiplexing speech signals. Analogue speech signals inputted from telephone sets 1a, 1b, --- to encoding means 800a, 800b, ---, respectively, are converted at first into digital speech signals in A/D converters 801. They are, then, outputted to a priority signal producing means 240, respective speech detectors 802 and respective PCM codes 803. Although a PCM coder is used here, it is not restricted thereto, but a coder by ADPCM, multi-pulse coding, APC, etc. may be used therefor as well. The output of the PCM coder 803 is sent to a packet assembler 804 and the output 220 of the speech detector 802 in each of the encoding means 800a, 800b, --- is supplied to the packet assembler 804, the priority signal producing means 204 and a header generator 850. The packet assembler 804 assembles a packet on the basis of the PCM speech unit signal 806 supplied by the PCM coder 803 and the header signal 805 supplied by the header generator 850, only for information corresponding to talk-spurts among the speech detection signals supplied by the speech detector 802. Packet selecting means 820 receives the packets 840 from the packet assemblers 804 in the encoding means 800a, 800b, --- along with a priority signal 330 supplied from the priority signal producing means 240 and information on the number of packets in an FIFO memory (queue) 821 and selects packets to be transmitted on the basis of the capacity of the transmission line T, which are outputted from the memory 821 to the transmission line T. On the other hand, packets received through the transmission line T are once accommodated in an FIFO memory (queue) 831 and distributed by packet distributing means 830 to packet disassemblers 813 for the

respective trunks in accordance with the addresses of the destination included in the packets. The packet disassembler 813 disassembles the distributed packet, verifies that sequence numbers are arranged in a predetermined order, and outputs speech information separated from the packet to a PCM decoder 812 with a timing specified by a time stamp. When there exists no speech information to be outputted, speech information corresponding to silence is outputted. Each of the PCM decoders 812 expands logarithmically compressed PCM signals and outputs them to a D/A converter 811. The D/A converter 811 outputs them to each of telephone sets 1 after having converted the digital signals into analogue signals.

The Examiner specifically cited col. 14, line 65,–col. 15, line 6, of Kondo et al. which states the following:

> "In this way, in the embodiment indicated in FIG. 8, when talk-spurt signals are concentrated and the number of packets within the FIFO memory (queue) is increased so that it is feared that buffer overflow may take place in a speech packet communication system, it is possible to discard packets in an effort to delete only those having small influences on the speech sound quality and thus to control the number of packets within the FIFO memory (queue) to minimize degradation of the speech sound quality."

The Examiner incorrectly concludes that it would have been obvious "to modify the teachings of Henley et al (5526353) in view of Shiono (4618936) with selective speech data discarding because it would allow for the removal of bad sound data as well as avoiding buffer overflow". This is a further unwarrented reconstruction and, in fact, is contrary to Shiono who specifically wants to avoid loss of data. Moreover, Kondo et al. are addressing a problem (multiplexing speech signals) that neither Henley et al. nor Shiono are considering, much less the claimed invention.

As to claim 3, the Examiner again relies on Henley et al. citing col. 15, lines 1 to 16, while quoting from claim 3. This is again misleading since it suggests that the quoted passage is to be found at the cited passage of the reference. In fact, what new claim 6, corresponding to claim 3, recites is "wherein

when said dummy code is input to said input means, said voice decoder means outputs digitalized digital voice data in which *the strength of said compressed voice code inputted immediately prior to said dummy signal is reduced*" (emphasis added). What Henley et al. states at col. 15, lines 6 to 12, is "Sample 5 further illustrates the circumstance when a shortened audio data sample 380 is transmitted. Sample 5, which is only 24 bytes long, is inserted into the receiving buffer at PI_5 =73. Since sample 5 is short by 20 bytes, the missing 20 bytes are filled with white noise, representing silence. The silence is not shown, as will be explained." This is quite different from what is disclosed and claimed by the present invention. Henley et al. are concerned with transmitting ATM packets. White noise is not what is input to the decoding buffer 301 by the insertion/disposal control unit 100. The dummy code input to the decoding buffer 301 is as a result of monitoring the data in the speaker output buffer 501, not the need to fill a packet in a packet switched system. There is no suggestion of inputting such a dummy code wherein "*the strength of said compressed voice code inputted immediately prior to said dummy signal is reduced*", as specifically recited in the claim.

Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over the patents to Henley et al., Shiono and Kondo et al., further in view of U.S. Patent No. 5,617,423 to Li et al. This rejection is also respectfully traversed for the reason that the combination of Henley et al., Shiono, Kondo et al. and Li et al. does not result in the claimed invention, nor is there any teaching that can be derived from this combination that would suggest the claimed invention.

The patents to Henley et al. Shiono and Kondo et al. have been distinguished above. Claim 4, as previously mentioned is directed to the embodiment shown in Figure 2 of the present application.

In making this rejection, the Examiner states that Henley et al. "does not *explicitly* teach echo component removal means". Again, the use of the adverb "explicitly" is misleading because it implies that there might be some *implicit* teaching in Henley et al. of this feature when, in fact, there is none. The Examiner

relies on Li et al. for a teaching of echo cancellation.

Li et al. disclose a personal communications system enables the operator to simultaneously transmit voice and data communication to a remote site. The personal communications system is equipped with two telephone line interfaces to allow connection between two remote sites. The connection between the first remote site and the local site may operate in a voice over data communications mode to simultaneously send compressed voice and data. A digital transmission protocol which is consistent with current packet standards is used to create an independent channel through use of a modified supervisory packet for negotiating communication parameters, including the speech compression algorithm, the speech compression ratio, the communication multiplex scheme, and other operations needed for control of remote hardware interfaces.

The Examiner specifically cites col. 30, lines 7–23, of Li et al. which states the following:

> "The echo canceler of FIG. 14 uses a least mean square (LMS) method of adaptive echo cancellation. The echo estimate signal subtracted from the incoming signal at 1403 is determined by function 1411. Function 1411 is a an FIR (finite impulse response) filter having in the preferred embodiment an impulse response which is approximately the length of delay though the acoustic path. The coefficients of the FIR filter are modeled and tailored after the acoustic echo path of the echo taking into account the specific physical attributes of the box that the speaker 304 and microphone 303 are located in and the proximity of the speaker 304 to the microphone 303. Thus, any signal placed on to the speaker is sent through the echo cancellation function 1411 to be subtracted from the signals received by the microphone 303 after an appropriate delay to match the delay in the acoustic path. The formula for echo replication of function box 1411 is:
>
> $$\hat{y}(n)=\sum_{i=0}^{N-1} h_i x(n-i)$$
>
> and the result of the subtraction of the echo cancellation signal $\hat{y}$ (n) from the microphone signal y(n) is
>
> $$e(n)=y(n)-\hat{y}(n).$$

The Examiner incorrectly concludes that it would have been obvious "to modify the teachings of Henley et al (5526353) in view of Shiono (4618936) in view of Kondo et al (4993022) with an echo cancellation feature because it would advantageously remove unwanted feedback and echo from the signal of interest", citing col. 7, lines 40–46, of the patent to Li et al. The cited passage states the following:

> "The digitized voice patterns are passed to the voice control circuit 306 where echo cancellation is accomplished, the digital voice signals are reconstructed into analog signals and passed through multiplexor circuit 310 to the telephone line interface circuit 309 for analog transmission over the telephone line. The incoming analog voice from the telephone connection through telephone connection circuit 309 is passed to the integral CODEC of the voice control circuit 306 where it is digitized. The digitized incoming voice is then passed to digital telephone CODEC circuit 305 where it is reconverted to an analog signal for transmission to the selected telephone interface (either the handset 301, the microphone/speaker 303/304 or the headset 302). Voice Control DSP circuit 306 is programmed to perform echo cancellation to avoid feedback and echoes between transmitted and received signals, as is more fully described below."

Since none of Henley et al., Shiono or Kondo et al. disclose systems where echo cancellation is desirable or needed, the combination of Li et al. with the other three references is, again, an unwarranted reconstruction that would not, in any event, produce the claimed invention.

In summary, the patentable novelty of the present invention resides in providing a special control feature of output digital voice data in a speaker buffer in such way that underflow of output digital voice data does not occur and a speaker output voice signal remains continuous. Additionally, the digital voice data is controlled to avoid overflow of the speaker buffer and thus accumulation of delays in the speaker output voice from the time of input from the transmission source terminal similarly does not occur. Thus, the controlling of the buffer data amount improves the quality of an audio signal from the speaker.

In view of the foregoing, it is respectfully requested that this amendment

be entered, that claims 5, 6 and 7 be allowed, and that the application be passed to issue. In the alternative, it is requested that this amendment be entered for purposes of appeal.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

C. Lamont Whitham
Reg. No. 22,424

Whitham, Curtis & Christofferson, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
Tel. (703) 787-9400
Fax. (703) 787-7557
Customer No.: 30 743